the signal from one of the plurality of signal streams coupled to the closed one of the first plurality of switches to substantially charge one of the plurality of signal buses which is also coupled to the closed one of the first plurality of switches and which is not currently being read at the output.--

A1 cont.

--33. The bus system as set forth in claim 32 wherein the control system controls when at least another one of the first plurality of switches is closed to allow the signal from another one of the plurality of signal streams coupled to the closed another one of the first plurality of switches to be read at the output from another one of the plurality of signal buses which is also coupled to the closed another one of the first plurality of switches.--

--34. The bus system as set forth in claim 32 further comprising a plurality of second switches, each of the plurality of second switches is coupled between one of the plurality of signal buses and the output, the control system controls when each of the of the plurality of second switches is closed to allow the signal on one or more of the plurality of signal buses to be read at the output.--

--35. The bus system as set forth in claim 32 wherein the control system provides binning by coupling the signals from two or more of the plurality of signals buses to be read at the output at substantially the same time to average the signals together.--

--36. The bus system as set forth in claim 32 wherein a pair of the plurality of signal buses are coupled to each of the plurality of signal streams for differential processing.--

--37. The bus system as set forth in claim 32 wherein the control system further comprises:

a decoder; and

a first control circuit coupled between the decoder and each of the first plurality of switches.--

--38. The bus system as set forth in claim 37 wherein the decoder is a sequential decoder.--

--39. The bus system as set forth in claim 37 wherein the decoder is a random decoder.--

--40. The bus system as set forth in claim 37 wherein the control system further comprises:

an address counter coupled to the decoder; and

a second control circuit coupled between the address counter and each of the second plurality of switches.--

--41. A method for transferring signals from a plurality of signal streams to an output, the method comprising:

reading at least one of the signals at an output from at least one of a plurality of signal buses, each of the plurality of signal buses is coupled to the output;

allowing at least another one of the signals to substantially charge at least another one of the plurality of signal buses that is not being read at the output while the one of the signals is being read; and

reading the at least another one of the signals at the output after the at least another one of the plurality of signal buses is substantially charged with the another one of the signals.--

--42. The method as set forth in claim 41 further comprising controlling when each of the plurality of signal buses is charged with one of the signals.--

--43. The method as set forth in claim 41 further comprising controlling when the reading at the output from each of the plurality of signal buses occurs.--

--44. The method as set forth in claim 41 wherein the reading at least one of the signals comprises binning the signals from two or more of the plurality of signals buses together to be read at the output at substantially the same time to average the signals together.--

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--45. The method as set forth in claim 41 wherein the reading further comprises differential processing of the signals read from a pair of the plurality of signal buses, wherein each of the pair of the plurality of signal buses are coupled to one of the plurality of signal streams.--

A1 concl'd

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--46. The method as set forth in claim 41 wherein the allowing at least another one of the signals to substantially charge at least another one of the plurality of signal buses comprises charging each of the plurality of signal buses with one of the signals in a sequential order.--

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--47. The method as set forth in claim 41 wherein the allowing at least another one of the signals to substantially charge at least another one of the plurality of signal buses comprises charging each of the plurality of signal buses with one of the signals in a random order.--

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--48. The method as set forth in claim 41 wherein the allowing at least another one of the signals to substantially charge at least another one of the plurality of signal buses comprises charging each of the plurality of signal buses with one of the signals at substantially the same time.--